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MCA-2

Seat No. _____

M. Sc. (ECI) (Sem. II) (CBCS) Examination

April / May - 2018

Paper - 6 : Advanced Digital Electronics

Time : $2\frac{1}{2}$ Hours] [Total Marks : **70**

1 Answer the following : (Any **7** out of 10) **2×7=14**

(1) Write the count sequence for MOD 4 Ring counter.

(2) List the types of Shift Registers.

(3) For presettable and clearable J–K FF with active high J-K inputs and active low preset–clear inputs, what would be the logic status of Q output when

(A) J = 1, K = 1, Preset = 1, Clear = 0

(B) J = 1, K = 0, Preset = 1, Clear = 1

(4) Write the number of flip flops required to construct

(A) MOD 6 Ring Counter

(B) MOD 12 Binary Counter

(C) MOD 12 Johnson Counter

(D) BCD Counter

(5) Give at least one IC type and number for each

(A) 8 bit D/A converter

(B) 4 bit binary ripple counter

(6) Write the truth table of S–R Flipflop. (Active high)

(7) Which are the inbuilt MODs in IC 74293?

(8) Write the PROS & CONS of Sigma–Delta A/D converter. (2 points each)

(9) State true or false :

(A) According to Nyquist theorem, the sampling rate should be at least twice of the input signal.

(B) Johnson counter always produces Square wave.

(10) Two T type flipflops are in cascaded arrangement. If the input frequency of FF1 is 10 MHz, what is the output frequency of FF2?

2 Answer the following : (Any **Two** out of Three from a, b, and c) **14**

(a) Explain FUSE and ANTIFUSE as some programmable interconnect technologies. **5**

(b) Draw block diagram of 12bit BCD input D/A converter. If the step size is 5mV, determine the full scale output. **5**

(c) Write the truth table of Full adder. Implement it using suitable PROM. **5**

(d) Compulsory question **4**

There is a Decimal to BCD priority encoder, active LOW(D_9 has the highest priority). The outputs are A,B,C where A = MSB and C = LSB. Determine the logic status of the output bits for the following cases :

(A) All inputs are in logic "0" states.

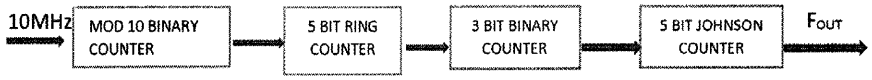
(B) D_1 to D_5 logic "0" states and D_6 to D_9 logic "1" states.

(C) D_9 is logic "0" states others are unknown.

(D) If the input bit stream is 1011011001, with extreme left is D_0 and extreme right is D_9.

3 Answer the following : **14**

(A) For the following multistage counters arrangement, explain and find the F_{OUT}. **5**



(B) Explain Flash type A/D converter in detail. **5**

(C) Write the difference between PLA and PAL. **4**

OR

(A) Explain in detail MOD 4 counter with decoding gates. **7**

(B) Explain in detail Master – Slave flipflop. **7**

4 Answer the following : **14**

(A) Design and explain R – S, Flipflop with active LOW inputs. **7**

(B) Draw the internal architecture of 16 × 4 PROM. **7**

5 Answer the following : (Any **Two** out of Four) **14**

(A) Explain the timing parameters of flipflop. **7**

(B) Design and explain 4 bit BI - DIRECTIONAL shift register. **7**

(C) Design and explain in detail 4 bit Johnson Counter. **7**

(D) Implement the following Boolean expression using PLA **7**

$F_1(A, B, C, D) = \sum(1, 2, 3, 6, 7, 11)$

$F_2(A, B, C, D) = \sum(4, 8, 9, 12, 13, 14)$
